ELECTRONICS ENGINEERING

Advanced Solid-State Circuit Design: Evolution of VCO-Based Modulators, High-Speed Serial Links, and Ultralow-Voltage SRAM Architectures

Published: October 16, 2026 | Index ID: #9

The landscape of integrated circuit (IC) design has undergone a radical transformation as CMOS technology scales into the deep-submicron and nanometer regimes. The **IEEE Journal of Solid-State Circuits (JSSC)** has long served as the primary repository for these breakthroughs, documenting the transition from traditional analog-intensive designs to digital-assisted and time-domain architectures. As supply voltages (V_{DD}) continue to scale downward to conserve power, particularly in Internet of Things (IoT) and mobile applications, engineers face the daunting task of maintaining signal integrity, speed, and dynamic range. This article provides a comprehensive technical analysis of several key advancements reported in JSSC Volumes 48 through 52, focusing on VCO-based continuous-time delta-sigma modulators (CT-DSMs), high-speed serial links reaching 66 Gb/s, and timing-speculative SRAM architectures.

The Shift to Time-Domain Processing: VCO-Based CT-DSMs

Traditional Continuous-Time Delta-Sigma Modulators (CTDSMs) rely heavily on high-gain Operational Transconductance Amplifiers (OTAs) to perform integration. However, in deep-scaled processes like 28nm and 16nm CMOS, the reduced intrinsic gain of transistors and limited voltage headroom make high-performance OTA design increasingly difficult. This has led to the rise of **VCO-based modulators**.

Mechanics of VCO-Based Quantization

A Voltage-Controlled Oscillator (VCO) inherently acts as both an integrator and a quantizer. The input voltage controls the frequency, and the phase of the oscillator represents the integral of that frequency. By sampling the phase (usually via a multi-phase output), the circuit performs quantization in the time domain. This architecture is particularly attractive because it is **mostly digital**, taking advantage of the superior time resolution of modern CMOS processes rather than struggling with limited voltage headroom.

Third-Order Noise Shaping and Stability

To achieve high dynamic range, higher-order noise shaping is required. Recent research, such as the work by Babaie-Fishani, explores mostly digital VCO-based CT-SDMs with **third-order noise shaping**. Achieving third-order shaping in a VCO-based loop typically requires a combination of an analog filter and the inherent integration of the VCO. The primary challenge here is the non-linearity of the VCO's voltage-to-frequency (V-to-F) conversion. Techniques such as **Digital Nonlinearity Correction (DNC)** or look-up table-based calibration are employed to mitigate the second and third-order harmonics that would otherwise degrade the Signal-to-Noise and Distortion Ratio (SNDR).

The OTA-less Advantage

OTA-less designs replace power-hungry analog integrators with passive RC networks or inverter-based integrators. By eliminating the OTA, the modulator benefits from:

- Reduced Power Consumption: Inverters scale better with process and voltage than traditional analog biases.
- Area Efficiency: Digital-centric designs occupy significantly less silicon area.

- Process Portability: Highly digital loops are easier to migrate to smaller nodes (e.g., from 65nm to 28nm).

Ultralow-Voltage SRAM and Timing Speculation

As operating voltages drop toward the sub-threshold or near-threshold regions (e.g., 0.4V to 0.6V), Static Random-Access Memory (SRAM) becomes the primary bottleneck for system-on-chip (SoC) reliability. The primary issues include **read-disturb**, **write-margin degradation**, and increased **process variation sensitivity**.

Double Sensing Schemes

One of the most effective methods to combat bitline (BL) swing limitations in ultralow-voltage SRAM is the **Double Sensing Scheme**. Traditional single-ended or differential sensing often fails due to the slow discharge of the bitline at low V_{DD}. A double sensing approach uses a preliminary sense-amplifier (SA) activation followed by a secondary verification or a reinforced sensing cycle. This ensures that even with significant bitline leakage and noise, the data state is captured correctly.

Selective Bitline Voltage Regulation

Selective Bitline Voltage Regulation involves dynamically adjusting the bitline pre-charge level based on the operation (read or write) and the specific physical location of the cell. By regulating the bitline voltage, designers can:

1. Improve the Static Noise Margin (SNM) during read operations.
2. Reduce Bitline Leakage, which is a major component of standby power in dense memory arrays.
3. Optimize the Write Trip Point, ensuring that data can be flipped even when the driving transistors are weak.

Timing Speculation and Error Detection

Timing speculation (often referred to as "Razor" techniques in logic) is applied to SRAM to allow the memory to operate at frequencies higher than the worst-case corner would dictate. If a timing violation occurs (i.e., the bitline does not discharge sufficiently before the sense amplifier fires), the system detects the error and initiates a recovery cycle. This allows for massive energy savings by operating at the "typical" rather than "worst-case" timing margins.

High-Speed Serial Links: Reaching 40-66 Gb/s

Data centers and high-performance computing (HPC) demand ever-increasing throughput. Serializer/Deserializer (SerDes) transceivers in the 40 Gb/s to 66 Gb/s range are now common, but they face extreme signal integrity challenges, including **Inter-Symbol Interference (ISI)** and **Channel Loss** (often >30 dB at Nyquist frequencies).

3-Tap Decision Feedback Equalization (DFE)

To recover data from a highly distorted channel, **Decision Feedback Equalizers (DFE)** are utilized. A 3-tap DFE specifically targets the first three post-cursor ISI components. The challenge at 66 Gb/s is the **feedback loop timing**. The DFE must decide the value of a bit and apply the correction to the next bit within one unit interval (UI), which at 66 Gb/s is approximately 15 picoseconds. This necessitates highly parallelized architectures and loop-unrolling techniques.

Multiphase Serialization

In the transmitter (TX), generating a clean 40+ Gb/s clock is difficult. **Multiphase serialization** allows the use of lower-frequency internal clocks (e.g., a quarter-rate 10 GHz clock for 40 Gb/s data) to shift bits onto the wire. This reduces the requirements on the Phase-Locked Loop (PLL) and helps manage clock distribution jitter, which is the

primary killer of the **Eye Diagram** at these speeds.

Comparative Analysis of Circuit Architectures

The following table compares different high-speed and low-power design strategies based on technical data from the JSSC publications mentioned in the study data.

Feature/Technology	VCO-Based CTDSM	High-Speed SerDes	Ultralow-Voltage SRAM
Primary Focus	Dynamic Range & Power Efficiency	Throughput & Signal Integrity	Reliability & Density
Key Challenge	V-to-F Nonlinearity	Channel Loss & Jitter	Process Variation & V_{th} Scaling
Process Node	28nm - 65nm CMOS	28nm - 65nm CMOS	Deep-submicron (Ultralow V_{DD})
Key Technique	Third-Order Noise Shaping	3-tap DFE / Multiphase TX	Double Sensing / Timing Speculation

Ultra-Low Power Analog Filter Integration

While digital circuits scale well, analog filters remain necessary for anti-aliasing and signal conditioning. The shift toward **Ultra Low-Power Low-Voltage Analog Integrated Filters** involves using non-traditional technologies such as **Bipolar-JFET** or sub-threshold CMOS. For instance, integrated filters operating at very low frequencies for biomedical applications must achieve high linearity while consuming only nanowatts of power. These designs often leverage **log-domain filtering** or **switched-capacitor** techniques tailored for low-leakage processes.

Technical Implementation: A Step-by-Step Guide to VCO-Based Modulator Design

Engineers looking to implement a mostly-digital VCO-based CTDSM should follow a structured design flow to ensure stability and performance:

Step 1: Loop Filter Optimization

Determine the required noise-shaping order. For third-order shaping, design a loop filter that integrates the error signal before it reaches the VCO. Passive RC filters are preferred in 28nm processes to avoid the headroom issues of active integrators.

Step 2: VCO Design and Phase Quantization

Select a ring oscillator topology for its wide tuning range and multi-phase outputs. The number of phases (N) determines the quantization noise level ($12 \times \log_2(N)$ improvement in SQNR). Ensure the VCO has sufficient KVCO (tuning sensitivity) to cover the signal swing but not so much that it becomes overly sensitive to power supply noise.

Step 3: Feedback DAC Design

The feedback Digital-to-Analog Converter (DAC) is the most critical component for linearity. Use **Data-Weighted Averaging (DWA)** to move DAC element mismatch noise to high frequencies. For CTDSMs, the DAC pulse shape (e.g., Non-Return-to-Zero or RZ) must be carefully controlled to minimize **Clock Jitter Sensitivity**.

Step 4: Digital Background Calibration

Implement a digital engine to track the VCO's V-to-F gain. Use a pseudo-random bit stream (PRBS) to identify nonlinearities and subtract them in the digital domain. This allows the use of a more power-efficient, albeit less linear, VCO.

Operational Failures and Troubleshooting in High-Speed Links

Designing transceivers at 40-66 Gb/s often results in unexpected failure modes during post-silicon validation. Below are common issues and their engineering solutions:

- Problem: Eye Closure due to Excessive ISI.
  Solution: Increase the DFE tap weight or introduce a Continuous-Time Linear Equalizer (CTLE) at the receiver front-end to provide high-frequency boost before the DFE.
- Problem: Resonances in the Package/PCB.
  Solution: Use differential signaling with tight impedance control and optimize the T-coil structures on the I/O pads to cancel parasitic capacitance (C_{pad}).
- Problem: PLL Reference Spurs.
  Solution: Implement a high-bandwidth loop filter and use a low-noise regulated power supply for the LC-VCO to prevent supply noise from modulating the clock phase.

Strategic Implications for the Semiconductor Industry

The research presented in JSSC Volumes 48 and 50 highlights a broader industry trend: the **digitization of analog** . As we move toward 3nm and beyond, the "art" of circuit design is shifting from achieving high gain and high linearity in single transistors to building robust, self-calibrating systems that use digital logic to compensate for analog imperfections.

This paradigm shift is particularly evident in the development of **Serializing Transmitters** and **VCO-based ADCs**. By moving the complexity into the digital domain, manufacturers can leverage Moore's Law to reduce costs and power. However, this places a higher burden on **Electronic Design Automation (EDA)**tools to accurately model the mixed-signal interactions and temporal noise that traditional tools might overlook.

In the realm of memory, the move toward timing-speculative SRAM and selective bitline regulation is essential for the survival of the 6T (six-transistor) SRAM cell. Without these innovations, the increase in V_{min} (minimum operating voltage) would prevent chips from scaling their power consumption in tandem with their logic density. The methodologies documented in the IEEE Journal of Solid-State Circuits continue to provide the roadmap for the next generation of energy-efficient, high-performance computing hardware, bridging the gap between theoretical physics and practical silicon implementation.